

IMPLEMENTATION ISSUES FOR CONGESTION CONTROL IN ATM NETWORKS

M.Marchese (*), F.Curatelli (+), M.Chirico (+), L.Mangeruca (+)

(*) DIST- University of Genova - Via Opera Pia, 13 - 16145 Genova
(+) DIBE- University of Genova - Via Opera Pia, 11A - 16145 Genova

Abstract

The design of Broadband Integrated Services Digital Networks (B-ISDN) requires the investigation of specific techniques to guarantee different Quality of Services (QoS) requirements for each traffic class in the network. In this context, a unified environment for the simulation and design of an ATM node is a useful approach to test the effectiveness and the implementation aspects of the techniques mentioned above. In this paper a complete ATM node has been modelled in VHDL in a modular and flexible way and critical computational aspects are investigated.

1. INTRODUCTION

In the telecommunications world, new services like videotelephony, videoconferencing, tele-teaching are currently being added to existing services like voice and low speed data. Due to the evolution of computer and transmission technologies, a very high transmission speed can be achieved; so, the support of different services by using a unified Broadband Integrated Sources Digital Network (B-ISDN), has become feasible. The transfer mode for the B-ISDN is called ATM. ATM is a connection oriented transfer mode where the information is packetised (in packets of fixed length named cells) and statistically multiplexed [1]. Due to the statistical multiplexing some mechanisms to protect the network from the congestion and to guarantee performance requirements are needed. ATM received a great deal of attention in the literature: many works addressed theoretical issues as in [2-8], among the others; other works took into account the implementation of an ATM switching element or of a generic building block of the future B-ISDN as in [9-10]. The widely treated issue of congestion and admission control presents many computational aspects not taken into account in a theoretical approach but surely to be considered both to get an efficient simulator and to obtain a real implementation of a congestion control strategy. Our paper presents an ATM node model and an admission control strategy, already in the literature [11]. The critical computational aspects of the theoretical model are carefully analysed and a complete ATM node is modelled in VHDL. The purpose of our work is to build an experimental bench to validate theoretical models of congestion control in ATM nodes through simulation, and to study hardware and software architectures well suited for the implementation of those models. In particular, the complete ATM node in VHDL has

been modelled by adopting a modular approach, so that different alternatives in the node architecture and functionality can be easily verified. Since the main purpose of the work is to study congestion control techniques, the other functions of the node, i.e. switching, are modelled at an high-level of abstraction in order to avoid unnecessary complications and to achieve a high simulation efficiency. The paper is organised as follows: Section 2 is dedicated to the description of the ATM node model and of the Call Admission Control (CAC) strategy. Section 3 is about the VHDL description of the ATM model, while the computational critical aspects of the control mechanism are focused in Section 4. Section 5 contains the Conclusions.

2. THE ATM NODE MODEL AND THE CAC SCHEME

The node model and the associated CAC scheme can be briefly summarised as follows.

The traffic in the network is divided into M classes, characterised by statistical parameters like peak and average transmission rate, as well as by QoS requirements, like cell loss and cell delay rate. The general structure of a node is depicted in Fig.1. A resource allocation scheme and a local control access rule of the type presented in [11] are implemented for every outgoing link, and their structure, also shown in the figure, will be briefly summarised in the following. Each traffic class is assigned a separate buffer whose output is statistically multiplexed on the outgoing link by a scheduler, which divides the global channel capacity C_T among the classes. Connection requests, are also processed on a class basis. Two controls are exerted on the system, by using a two level hierarchical control scheme, one acting on the scheduler and the other on the call admission. At the higher level of the hierarchical control scheme, a bandwidth allocation controller periodically reassigns capacity partitions to every class. The scheduler receives the values of the partitions and must assure that every buffer is assigned a percentage of slots equal to the ratio between the total capacity and the capacity assigned to its class. The capacity partitions $V_m^{(h)}$ $h = 1, \dots, M$, are computed by the controller at discrete time instants $m = 0, K, 2K, \dots$ (K is the length of the intervention period in slots), based on the minimisation of a cost function that takes into account the overall cell loss probability. At the lower level, M access controllers decide about the

acceptance of a connection request, independently for each class. The packet loss rate and the rate of cells exceeding a delay requirement for the connections of one class over an outgoing link can be computed [11]. The acceptance decisions are taken on the basis of the two above mentioned quantities, and therefore depend on the capacity currently allocated to the class, on the current number of connections in progress, and on the statistical characteristics of the specific traffic. Class h traffic is supposed to be made up by bursty connections with identical and statistically independent characteristics. We indicate with $b^{(h)}$, $B^{(h)}$, and $P^{(h)}$ the burstiness, the average burst length, and the peak bit rate, respectively, of the h -th class. Sources are supposed to be of the ON-OFF type, and are modelled simply as a two state (idle and active, respectively) Markov chain.

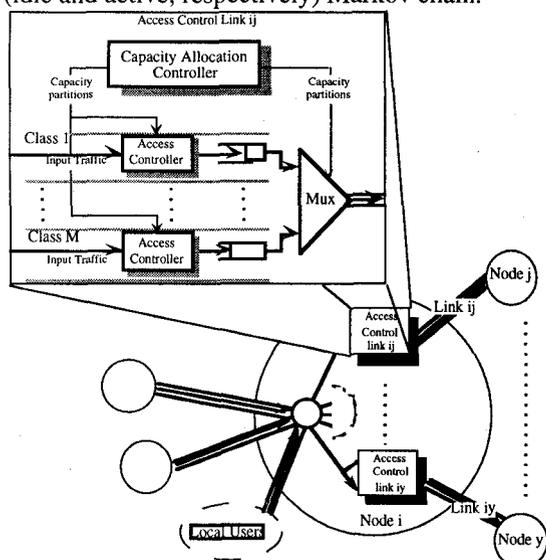


Figure 1. Structure of the node.

After every access controller receives its capacity assignment from the bandwidth allocation controller, it computes the maximum number of connections of the h -th class that can be supported on link ij as

$$N_{ij}^{(h)}(m) = \min\{N_{ij,L}^{(h)}(m); N_{ij,D}^{(h)}(m)\} \quad (1)$$

where $N_{ij,L}^{(h)}(m)$ is the maximum number of connections on the link capable of maintaining the cell loss rate $R_{loss}^{(h)}(N, Q)$ below a given upper bound $\epsilon^{(h)}$, being N the number of active calls and Q the dimension of the buffer. In formula, not considering the time m to simplify the notation:

$$N_{ij,L}^{(h)} = \max_N \{N : R_{loss}^{(h)}(N, Q) \leq \epsilon^{(h)}\} \quad (2)$$

$N_{ij,D}^{(h)}(m)$ is the maximum number of connections computed by imposing a similar limit on cell delay $R_{delay}^{(h)}(N, Q)$, namely, that the probability of

exceeding a delay of $D^{(h)}$ slots be less than an upper bound $\delta^{(h)}$:

$$N_{ij,D}^{(h)} = \max_N \{N : R_{delay}^{(h)}(N, Q) \leq \delta^{(h)}\} \quad (3)$$

Summing up, the local acceptance rule is: a new connection of the h -th class arriving at time slot k , $m+D \leq k \leq m+D+K-1$ (where D indicates the number of slots required for the computations), is accepted on link ij if

$$N_{ij,A}^{(h)}(k) + 1 \leq N_{ij}^{(h)}(m) \quad (4)$$

where $N_{ij,A}^{(h)}(k)$ is the number of connections of the h -th class in progress at time slot k .

A detailed theoretical description is not the aim of this paper but some details will be reported because the investigation of critical computation points is an important topic of the paper. In fact, in this paper, the theoretical description of the model is constantly associated with the details of the VHDL implementation, and parts of the code are also reported where needed for a good comprehension of the paper.

3. VHDL MODELLING AND SIMULATION

In this Section, part of the model mentioned above is spread and described by using the VHDL. A part of the ATM package, containing type definitions, constant declarations and functions used in the VHDL specifications, is illustrated in Figure 2.

Even the function R_{loss} , mentioned in the previous Section, is included in the ATM package. It represents a control system critical aspect and is the object of the next Section. The whole system is characterised in terms of the supported services, defined by means of the enumeration type class_type. Every constant associated to a specific service class is defined by using a constant array, so that parametrised descriptions can be easily specified. User cells and signalling are represented by means of records, as shown in Figure 1. The cell record is an abstraction of the information contained in each cell header, relevant to admission control. In particular each cell is uniquely identified by the node input link where the cells come from, the cell traffic class, and the connection which generated the cell, specified by means of the connection_id field.

The complete description of the ATM node is complex and it would require a large amount of space. In Fig. 3, the description of the ATM system is reported. It contains the traffic generators ('traffic_source') and the ATM node ('atm_node'). In a similar way each component of the ATM node is described in a hierarchical way. The ATM node is composed by a 'switch' and an 'out_stage'; this latter by two other components like 'congestion controller' and 'MUX' (which can be directly matched in Fig. 1). The congestion controller is divided into two parts: the access controller (with

the acceptance mechanism) and the bandwidth allocation strategy, with the computation of the maximum number of acceptable calls, and the computation of the bandwidth partitions for each traffic class. The bandwidth allocation is an actual critical computational aspect of the mechanism and will be the object of further research. In this paper, a part of the control mechanism, the computation of the cell loss rate, is described in detail and analysed.

```

package atm is
  type class_type is (TELEPHONE, VIDEO,
SLOW_DATA, FAST_DATA);
  type real_class_array is array (traffic_class) of real;
  type natural_class_array is array (traffic_class) of
natural;
  -- constants
  constant PEAK_BAND: real_class_array :=
      (TELEPHONE => 0.064,
       VIDEO => 150.0,
       ..... );
  .....
  -- cell and signalling types
  type cell_rec is record
    link : natural;
    class : class_type;
    connection_id : natural;
  end record;
  type signalling_message is (conn_req, conn_ack,
conn_end);
  type signalling_message is record
    link : natural;
    class : class_type;
    connection_id : natural;
    message : signalling_message;
  end record;
  .....
end atm;

```

Figure 2. The ATM package

```

entity atm_system is
end atm_system
architecture arc of atm_system is
signal conn_req: res_conn_req_rec;
signal conn_ack: conn_req_rec;
signal cells: res_cell_rec;
signal conn_end: res_cell_rec;
component traffic_source
  generic (seed: real);
  port (X1: inout res_conn_req_rec;
        X2: in conn_req_rec;
        X3: inout res_cell_rec;
        X4: inout res_cell_rec);
end component;
.....
end arc;

```

Figure 3. The ATM system

4. COMPUTATIONAL CRITICAL ASPECTS DESCRIPTION

In this Section critical computational aspects are focused and analysed. The details of the cell loss rate $R_{loss}^{(h)}(N, Q)$ computation are reported. The definition of some quantities is needed:

$$r_{loss}^{(h)}(n, Q) = \sum_{i=0}^Q \frac{\sum_{j=0}^n \max(i+j-Q, 0) f_j^{(h)}(n)}{n\Gamma} \pi_i^{(h)} \quad (5)$$

where $f_j^{(h)}(n)$ is the probability of having j connections of traffic class h generating a cell with n connections of the same class in the active state, that is

$$f_j^{(h)}(n) = \begin{cases} 0 & j < 0 \\ \binom{n}{j} (\Gamma^{(h)})^j (1 - \Gamma^{(h)})^{n-j} & 0 \leq j \leq n \end{cases} \quad (6)$$

and

$$n\Gamma = \sum_{j=0}^n j f_j^{(h)}(n) \quad (7)$$

The quantities $\pi_i^{(h)}$ in (5) represent the probability of having i cells in the buffer and are computed by using the transition matrix $G^{(h)}$, whose elements $g_{ij}^{(h)}(n, Q)$ represent the probability of transition from the state where i cells are queued in the k -th slot to the state where j cells are queued in the $(k+1)$ -th slot, given n active connections. The calculation of $g_{ij}^{(h)}(n, Q)$ is made by using the AF (Arrivals First) policy to model the process of simultaneous arrivals and departures in the queue [11]. Thus, we obtain

$$g_{ij}^{(h)}(n, Q) = \begin{cases} 0 & j < i-1 \\ f_{j-i+1}^{(h)}(n) & i \leq j < Q-1 \quad i \neq 0 \\ \sum_{s=Q-i}^n f_s^{(h)}(n) & j = Q-1 \\ f_0^{(h)}(n) + f_1^{(h)}(n) & j = 0 \\ f_{j+1}^{(h)}(n) & 0 < j < Q-1 \\ \sum_{s=Q}^n f_s^{(h)}(n) & j = Q-1 \end{cases} \quad (8)$$

$$g_{0j}^{(h)}(n, Q) = \begin{cases} f_0^{(h)}(n) + f_1^{(h)}(n) & j = 0 \\ f_{j+1}^{(h)}(n) & 0 < j < Q-1 \\ \sum_{s=Q}^n f_s^{(h)}(n) & j = Q-1 \end{cases} \quad (9)$$

(with $\sum_a^b \equiv 0$ if $a < b$)

The distribution

$$\Pi^{(h)} = [\pi_0^{(h)}, \pi_1^{(h)}, \dots, \pi_Q^{(h)}] \quad (10)$$

for the queue length can be obtained by solving the following set of linear equations:

$$\Pi^{(h)} = \Pi^{(h)} A^{(h)} \quad (11)$$

$$\sum_{i=0}^Q \pi_i^{(h)} = 1 \quad (12)$$

where the elements $g_{ij}^{(h)}(n, Q)$ of the state transition matrix $G^{(h)}$ are defined above.

Our aim, however, is to compute the cell loss rate $R_{\text{loss}}^{(h)}(N^{(h)}, Q)$ in the multiplexer. Being

$$v_n^{N^{(h)}} = \binom{N^{(h)}}{n} \left(\omega_a^{(h)} \right)^n \left(\omega_i^{(h)} \right)^{N^{(h)}-n} \quad (13)$$

the probability of having only n active connections out of $N^{(h)}$ connections in the system, the cell loss rate can be computed as

$$R_{\text{loss}}^{(h)}(N^{(h)}, Q) = \sum_{n=0}^{N^{(h)}} r_{\text{loss}}^{(h)}(n, Q) v_n^{N^{(h)}} \quad (14)$$

As it can be noted by analysing (14) and (5), the computation is performed by using two looped sums, which are really critical for a real-time computation as needed in a fast network as B-ISDN is. In Table 1, some computational values of (14) (in ms) are shown, by varying the number of accepted connections N and the allocated bandwidth V , for the traffic classes whose parameters are indicated below:

$P^{(1)}=1$ Mbit/s; $P^{(2)}=2$ Mbits/s; $P^{(3)}=10$ Mbits/s

$b^{(1)}=2$; $b^{(2)}=5$; $b^{(3)}=10$

$B^{(1)}=100$; $B^{(2)}=500$; $B^{(3)}=1000$ cells

$Q^{(1)}=20$; $Q^{(2)}=15$; $Q^{(3)}=10$ cells

Two values of bandwidth have been chosen to represent a traffic class, namely a "medium" ($V=50$) and an "extreme" ($V=150$) value. The computation has been carried out on a Sun Sparc10 workstation. Even if the results might seem acceptable at a first look, it has to be thought that this computation (14) has to be repeated many times to obtain the maximum number in (2) and (3). So, the introduction of an hardware accelerator to implement this function may be feasible.

At the moment the complete system at behavioural level has been described by using VHDL. Some software synthesis techniques have been utilised to get a VHDL code aimed at synthesising, from a VHDL code used for simulation tests. The utilised techniques have allowed to solve some typical

problems of a VHDL behavioural description like process communication and timing constraint management.

5. CONCLUSIONS

In this paper a complete VHDL model of an ATM node and of a Call Admission Control (CAC) scheme at behavioural level has been presented. Critical points of the control algorithm are investigated. The model introduced is useful both to simulate the behaviour of the node, and to provide a future path towards the real implementation of CAC mechanisms inside ATM nodes.

REFERENCES

- [1] M. de Prycker, *Asynchronous Transfer Mode, Solution for Broadband ISDN*, II Ed., Ellis Horwood, 1993.
- [2] G.M. Woodruff, R. Kositpaiboon, "Multimedia traffic management principles for guaranteed ATM network performance", *IEEE J. Select. Areas Commun.*, vol. 8, n. 3, April 1990.
- [3] Y. Takagi, S. Hino, T. Takahashi, "Priority assignment control of ATM line buffers with multiple QOS classes", *IEEE J. Select. Areas Commun.*, vol. 9, pp. 1078-1092, Sept. 1991.
- [4] J.A. Suruagy Monteiro, M. Gerla, "Bandwidth allocation in ATM networks", *Annals of Operations Research*, vol. 49, pp. 25-50, 1994.
- [5] I. Gün, V.G. Kulkarni, A. Narayanan, "Bandwidth allocation and access control in high speed networks", *Annals of Operations Research*, vol. 49, pp. 161-183, 1994.
- [6] H. Saito, *Teletraffic Technologies in ATM Networks*, Artech House, Inc., Norwood, MA, 1994.
- [7] R.O. Onvural, *Asynchronous Transfer Mode Networks: Performance Issues*, Artech House, Inc., Norwood, MA, 1994.
- [8] D. Hong, T. Suda, "Congestion control and prevention in ATM networks", *IEEE Network Mag.*, vol. 5, no. 4, pp. 10-16, July 1991.
- [9] P. Barri, J.A.O. Goubert, "Implementation of a 16 to 16 Switching Element for ATM Exchanges", *IEEE JSAC* vol. 9, no. 5, pp. 751-757, June 1991.
- [10] C.A. Johnston, H.J. Chao, "The ATM Layer Chip: An ASIC for B-ISDN Applications", *IEEE JSAC* vol. 9, no. 5, pp. 741-750, June 1991.
- [11] R. Bolla, F. Danovaro, F. Davoli, M. Marchese "An integrated dynamic resource allocation scheme for ATM networks", *Proc. Infocom '93*, San Francisco, CA, March 1993, vol. 3, pp. 1289-1297.

	No. of accepted connections (N)	Allocated bandwidth (V)	Computational time (ms)
Class 1	77	50	40
Class 1	259	150	280
Class 2	70	50	20
Class 2	271	150	240
Class 3	10	50	10
Class 3	59	150	20

Table 1. Computational time values for the evaluation of equation (14) (cell loss rate).